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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,283	11/19/2003	Bo Huang	10559-886001	1064

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EXAMINER	
DARE, RYAN A	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,283	HUANG ET AL.	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-23-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The corrections made to claims 10-12 on 3/23/06 overcome the corresponding claim objections.

Claim Rejections - 35 USC § 101

2. Claims 27-30 were amended on 3/23/06 to exclude non-statutory electronic signals, and the corresponding claim rejections under 35 U.S.C. 101 are withdrawn.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8, 10-20 and 22-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Bik et al., US PG Pub 2004/0006667, hereafter "Bik".

3. With respect to claim 1, Bik teaches a method comprising:

converting memory access instructions in a source code into standard formatted memory access instructions, in par. 31.

generating partitions containing the standard formatted memory access instructions, in par. 31.

generating a match set, the match set including matches of instruction patterns to the standard formatted memory access instructions in the partitions, in par. 31; and

transforming the matches to vector memory access instructions, in par. 31.

4. With respect to claim 2, Bik teaches the method of claim 1 in which converting comprises converting memory access instructions that read or write less than a minimum data access unit (MDAU) to memory access instructions that read or write a multiple of the minimum data access unit, in par. 4.

5. With respect to claim 3, Bik teaches the method of claim 2 in which converting further comprises transforming the memory access instructions that read or write the multiple of the minimum data access unit to a format including a base address plus an offset, in par. 59, with reference to figure 3A.

6. With respect to claim 4, Bik teaches the method of claim 1 in which generating partitions comprises:

generating a data flow graph containing basic blocks including the memory access instructions, in the data flow chart of figs. 10-19; and

for each basic block, applying a set of rules, in figs. 10-19.

7. With respect to claim 5, Bik teaches the method of claim 4 in which applying comprises limiting a subnode of a partition to memory access instructions directed to a specific memory bank, in fig. 10. The memory access instructions are directed to adjacent locations, and therefore the same bank.

8. With respect to claim 6, Bik teaches the method of claim 5 in which applying further comprises limiting the subnode of a partition to a memory read or a memory write, in pars. 82 and 85.

9. With respect to claim 7, Bik teaches the method of claim 5 in which the memory bank is a static random access memory (SRAM), in par. 44, line 6.

10. With respect to claim 8, Bik teaches the method of claim 5 in which the memory bank is a dynamic random access memory (DRAM), in par. 44, lines 6-7.

11. With respect to claim 10, Bik teaches the method of claim 5 in which the memory bank is an EEPROM, in par. 40, lines 12-13.

12. With respect to claim 11, Bik teaches the method of claim 5 in which the memory bank is a flash memory, in par. 40, line 13.

13. With respect to claim 12, Bik teaches the method of claim 5 in which the memory bank is a NVRAM, in par. 40, line 13 where a flash memory is a type of NVRAM.

14. With respect to claim 13, Bik teaches the method of claim 1 in which the instruction patterns comprise a pattern describing instruction semantics, in par. 31.

15. With respect to claim 14, Bik teaches the method of claim 1 in which the vector memory access instructions comprise single memory access instructions representing multiple memory accesses to a type of memory, in par. 31.

16. With respect to claim 15, Bik teaches a compilation method comprising:

converting memory access instructions that read or write less than a minimum data access unit (MDAU) to memory access instructions that read or write a multiple of the minimum data access unit, in par. 4.

converting the memory access instructions into a format including a base address plus an offset, in par. 59, with reference to figure 3A.

grouping subsets of the converted memory access instructions into partitions, in par. 31; and

vectorizing the converted memory access instructions in the subsets that match instruction patterns, in par. 31.

17. With respect to claim 16, Bik teaches the compilation method of claim 15 in which grouping comprises:

generating a data flow graph containing basic blocks including memory access instructions, in the data flow chart of figs. 10-19; and

generating subnodes in partitions, the subnodes including memory access instructions directed to a memory bank and performing the same operations, in fig. 10. The memory access instructions are directed to adjacent locations, and therefore the same bank.

18. With respect to claim 17, Bik teaches the compilation method of claim 16 in which the operation is a read, in par. 82.

19. With respect to claim 18, Bik teaches the compilation method of claim 16 in which the operation is a write in par. 85.

20. With respect to claim 19, Bik teaches the compilation method of claim 16 in which the memory bank is a static random access memory (SRAM), in par. 44, line 6.

21. With respect to claim 20, Bik teaches the compilation method of claim 16 in which the memory bank is a dynamic random access memory (DRAM), in par. 44, lines 6-7.

22. With respect to claim 22, Bik teaches the compilation method of claim 16 in which the memory bank is an EEPROM, in par. 40, lines 12-13.

23. With respect to claim 23, Bik teaches the compilation method of claim 16 in which the memory bank is a flash memory, in par. 40, line 13.

24. With respect to claim 24, Bik teaches the compilation method of claim 16 in which the memory bank is a NVRAM, in par. 40, line 13 where a flash memory is a type of NVRAM.

25. With respect to claim 25, Bik teaches the compilation method of claim 15 in which the instruction patterns comprises instruction semantics, in par. 31.

26. With respect to claim 26, Bik teaches the compilation method of claim 25 in which the instruction semantics comprises segments, in par. 31.

27. With respect to claims 27, 28, and 29, Applicant claims a computer program product that performs the method of claims 1, 2 and 3, respectively, and are therefore rejected using similar logic.

28. With respect to claim 30, Applicant claims the computer program product of claim 27, embodying the compilation method of claim 16 and is therefore rejected using similar logic.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

31. Claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bik. as applied to claims 1-8, 10-20 and 22-30 above, in view of the Microsoft Press Computer Dictionary, hereafter Microsoft.

32. With respect to claim 9, Bik teaches all parent claims as discussed above, but fails to expressly teach that the memory can be a scratchpad memory.

33. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the invention using a scratchpad memory because a scratchpad memory is high-speed, thus allowing for rapid retrieval of small items of data, as taught by Microsoft on page 421, under the definition of scratchpad.

34. With respect to claim 21, Bik teaches the limitations of all parent claims as discussed supra, and is rejected using similar logic as claim 9 above.

Response to Arguments

35. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar memory access instruction vectorization methods.

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Dare
June 12, 2006

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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